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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/752,944	12/28/2000	Geoffrey Francis Burns	US000413	9236

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EXAMINER	
MANNING, JOHN	
ART UNIT	**PAPER NUMBER**
2614	

DATE MAILED: 03/24/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/752,944	BURNS, GEOFFREY FRANCIS	
	Examiner	Art Unit	
	John Manning	2614	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *12/28/2000*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-7* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-7* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1-2 and 7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Toyoda et al (US Pat No 5,502,512) in view of Divine et al. (US Pat No 6,081,783).

In regard to claim 1, Toyoda discloses an apparatus and method for digital video and audio processing with information input and output processing devices (See Abstract). The claimed limitation of "communication means (101,102) for receiving data into the unit, transmitting data from the unit" is met by Figure 1, Item 107a. "107a is an input terminal for entering the video or audio information into the bus means 107, and 108, 109, and 110 are output means" (Col 2, Lines 61-64). The claimed limitation of a "first domain processing means (103) for first processing data depending on first domain configuration information" is met by Figure 1, Item 101. "In FIG. 1, numerals 101, 102, and 103 are information input and output processing means for entering video or audio information, and putting out directly or after arithmetic processing of video or audio information" (Col 2, Lines 49-52). The claimed limitation of a "second domain processing means (110) for second processing the first processed data depending second domain configuration information, the second processing being different than the first processing" is met by Figure 1, Item 102. "In FIG. 1, numerals 101, 102, and

103 are information input and output processing means for entering video or audio information, and putting out directly or after arithmetic processing of video or audio information" (Col 2, Lines 49-52). With respect to the second processing being different that the first processing, Toyoda discloses that the process to be executed by the "domains" is controlled by the control means 105. Both domains are operable to perform different functions or processes. "The operations of the information input and output processing means 101, 102, and 103 are controlled by the control means 105 in which the control information is entered from the input means 106" (Col 4, Lines 31-34). The claimed limitation of "a global control processor (120) connected to the communication means for providing the first domain configuration information and the second domain configuration information through the configuring first and second domains" is met by Control means 105. Toyoda fails to explicitly disclose the concept of the first and second "domains" having multiple processors as detailed in the claimed limitations of "the first processing means including multiple first domain processors (105-108) each connected communication means for receiving data and transmitting data communication means including transmitted between processors, first domain processor to first process the data, first domain processors including a first domain control processor controlling first processing the first domain" and "the second processors (111-115) each connected means for receiving data and processors, second domain processor differently sub- processing the data in order second process the data, the second domain processors including a second domain control processor controlling the second processing of the second domain". Divine teaches the concept of using

multiple processors in a particular "domain" so as to improve the overall speed and efficiency. "The maximum efficiency of complex single digital signal processors is also substantially limited. According to the principles of the present invention, an audio decoder can be constructed and operated which can process an audio data received in differing formats, stream with substantially greater speed and efficiency" (Col 2, Lines 41-46). Consequently, it would have been obvious to one of ordinary skill in the art to modify Toyoda with the first and second "domains" having multiple processors so as to improve the overall speed and efficiency.

In regard to claims 2 and 7, the claimed limitations of "the communication means include a stream-based communication means (101) connected to the global control processor and connected to a plurality of the processors of the first and second domains including the first and second domain control processors for transmitting information streams between connected processors" and "the stream-based communications means are connected to an input/output bus (120) to at times receive stream of data into the multi-processor unit through the stream-based communications means in to one of the connected processors and to at other times transmit a stream of data from one of the connected processors through the stream-based communications means onto the input/output bus" are met by the bus means 107 of Figure 1. "Concerning other operations, actions can be freely set in the information input and output processing means 101, 102, and 103 by the control means 105, for example, the video or audio information is fed in or sent out of the bus means 107 or the outside, or entered from the input terminals 101a, 102a, and 103a, and the bus means 107 or the

information input and output processing means in the previous stage, or the internally generated video or audio information is operated and processed" (Col 3, Lines 16-24). The combination of Toyoda and Divine both explicitly and implicitly discloses the use of memory; the combination fails to explicitly disclose blocks of memory with the selective interconnection to the plurality of processors. The examiner takes Official Notice that it is notoriously well known in the art to use multiple memory blocks with an arbitrator using indicator and addresses so as to increase the speed and efficiency of the memory. Consequently, it would have been obvious to one of ordinary skill in the art to the aforementioned combination with multiple memory blocks with an arbitrator using indicator and addresses so as to increase the speed and efficiency of the memory. The claimed limitation of "the control of the domain control processors during operation includes data flow control so that receiving a data object through the stream-based communication means triggers processing by the domain control processor" is met by Items 105 and 107 of Figure 1. "This control is entered into the control means 105 through the input means 106, and the control means 105 controls the information input and output processing means 101, 102, and 103 through the bus means 107" (Col 3, Lines 25-28). Furthermore, "the operations of the information input and output processing means 101, 102, and 103 are controlled by the control means 105 in which the control information is entered from the input means 106. Herein, the bus means 107 equivalently connects the information input and output processing means 101, 102, and 103, and the control means 105, and transmits video information, audio information and control information between them" (Col 4, Lines 31-38). The claimed limitation of "within

the domains, control of the processors includes direct control by the domain control processor by control signals provided directly through control lines (150,151) to the other domain processors from the domain control processor" is also met by Items 105 and 107 of Figure 1. "This control is entered into the control means 105 through the input means 106, and the control means 105 controls the information input and output processing means 101, 102, and 103 through the bus means 107" (Col 3, Lines 25-28). Furthermore, "the operations of the information input and output processing means 101, 102, and 103 are controlled by the control means 105 in which the control information is entered from the input means 106. Herein, the bus means 107 equivalently connects the information input and output processing means 101, 102, and 103, and the control means 105, and transmits video information, audio information and control information between them" (Col 4, Lines 31-38). The aforementioned combined teaching fails to explicitly disclose the use of a periodic sequencer. However, the examiner takes Official Notice that it is notoriously well know in the art to use a periodic sequencer so as to require less circuitry, thereby reducing cost and power consumption. Consequently, it would have been obvious to one of ordinary skill in the art to modify the aforementioned combined teaching with a periodic sequencer so as to require less circuitry, thereby reducing cost and power consumption. The aforementioned combined teaching fails to disclose that the processing includes FFT, IFFT, equalization, or forward error correction. The examiner takes Official Notice that it is notoriously well known in the art to signal processing techniques, such as FFT, IFFT, equalization, or forward error correction so are to transform the signal from one type to another.

Consequently, it would have been obvious to one of ordinary skill in the art to modify the aforementioned combined teaching with signal processing techniques, such as FFT, IFFT, equalization, or forward error correction so are to transform the signal from one type to another. Each of the "domains" are operable to process different types of data, which make structural difference between "domains" inherent. The disclosed "domains" process or transform information from one form to another. The first domain may process/transform or decode video, whereas the second domain may process/transform or decode video, thereby decoding on different transmissions standards. The aforementioned combined teaching fails to disclose that the system can decode an 8-VSB signal based on the ATSC standard or decode a COFDM transmission based on the DVB-T standard. However, it is submitted that it would have been clearly obvious to one of ordinary skill in the art to implement the aforementioned combined teaching with means to decode an 8-VSB signal based on the ATSC standard or decode a COFDM transmission based on the DVB-T standard so as to enable interoperability.

3. Claims 3-6 are rejected under 35 U.S.C. 103(a) as being unpatentable over Toyoda et al. in view of Divine et al. and further in view of Integrated Circuits and Microprocessors by R.C. Holland.

In regard to claim 3, the aforementioned combined teaching fails to explicitly disclose system implantation on an integrated circuit chip. Holland teaches the use of integrated circuits so as to provide a enhance performance, reduce power consumption, increased reliability, to reduce cost. The claimed limitation of "a substrate (301) of semiconducting material with different portions having different levels impurities" is met

by Figure 1.3 of Holland. The silicon substrate is a semiconducting material, where the n-type and p-type regions represent different levels of impurities. The claimed limitation of "a layer of insulation (302,303) on the semiconductor substrate" is met by the silicon substrate of Figure 1.3. The undoped region of the silicon substrate is an insulator because silicon in its intrinsic (i.e. not doped) is an insulator. The claimed limitation of "layer of wiring (304,305) including connection pads for flip-chip or circuit board; and wire-bond connection to (306,307)" is met by the connector leads of Figure 1.3. The connector lead and electrical contact for interconnection of transistor in an integrated circuit. Consequently, it would have been obvious to one of ordinary skill in the art to implement the combined teaching on an integrated circuit so as to provide a enhance performance, reduce power consumption, increased reliability, to reduce cost.

In regard to claim 4, the recitation a set top box has not been given patentable weight because the recitation occurs in the preamble. A preamble is generally not accorded any patentable weight where it merely recites the purpose of a process or the intended use of a structure, and where the body of the claim does not depend on the preamble for completeness but, instead, the process steps or structural limitations are able to stand alone. See *In re Hirao*, 535 F.2d 67, 190 USPQ 15 (CCPA 1976) and *Kropa v. Robie*, 187 F.2d 150, 152, 88 USPQ 478, 481 (CCPA 1951). The claimed limitation of "circuit board substrate (311)"is met by Figure 1.3 of Holland. The silicon substrate is a semiconducting material, where the n-type and p-type regions represent different levels of impurities.The claimed limitations of "a wiring layer (312) including connection pads circuit board substrate integrated circuit chip", "the integrated circuit

chip (300) of claim 3 mounted on the circuit board substrate" and" and "flip-chip or wire-bond connections (313,314) between connection pads integrated circuit chip and the connection pads the wiring layer." are met by Figure 1.3.

In regard to claim 5, the claimed limitation of "a connection (321) for receiving a channel encoded multimedia signal" is met by Item 106 of Figure 1 of Toyoda. The claimed limitation of "a connection (322) for transmitting a channel decoded multimedia signal" is met by Item 108 of Figure 1. The claimed limitation of "the circuit board assembly (310) of claim 4 for decoding the encoded multimedia signal to provide the decoded multimedia signal" is met by that discussed above for claim 4. A power supply is inherent to the reference.

In regard to claim 6, the recitation a digital television has not been given patentable weight because the recitation occurs in the preamble. A preamble is generally not accorded any patentable weight where it merely recites the purpose of a process or the intended use of a structure, and where the body of the claim does not depend on the preamble for completeness but, instead, the process steps or structural limitations are able to stand alone. See *In re Hirao*, 535 F.2d 67, 190 USPQ 15 (CCPA 1976) and *Kropa v. Robie*, 187 F.2d 150, 152, 88 USPQ 478, 481 (CCPA 1951). A source for providing a channel encoded multimedia signal is inherent to the reference. The claimed limitation of "the circuit board assembly (310) of claim 4 for decoding the encoded multimedia signal to provide the decoded multimedia signal" is met by that discussed above for claim 4. A power supply is inherent to the reference.The combined teaching fails to explicitly disclose a display and speakers. However, it is submitted that

it would have been clearly obvious to one of ordinary skill in the art to implement the combined teaching with a display and speakers so as to allow the user to see and hear the multimedia signals.

Conclusion

4. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure as follows:

- Garde et al. (US Pat No 5,685,005) discloses a digital signal processor configured for multiprocessing.
- Botsford, III et al. (US Pat No 5,646,687) discloses a temporally pipelined predictive encoder/decoder circuit and method.
- Allen et al. (US Pat No 5,583,500) discloses a method and apparatus for parallel encoding and decoding of data.
- Gove et al. (US Pat No 5,471,592) discloses a multi-processor with crossbar link of processors and memories and method of operation.
- Hoogenboom et al. (US Pat No 5,675,387) discloses a method and apparatus for efficient addressing of DRAM in a video decompression processor.
- Girod et al. (US Pat Pub No 2003/0072370) discloses a method and apparatus for providing scalable pre-compressed digital video with reduced quantization based artifacts.
- Shadwell et al. (US Pat No 6,542,203) discloses a digital receiver for receiving and demodulating a plurality of digital signals.

- Alvarez, II et al. (US Pat No 6,484,220) discloses a transfer of data between processor in a multi-processor system.
- Ohki et al. (US Pat No 5,666,169) discloses a parallel processor apparatus having means for processing signals of different lengths.
- Burns et al. (US Pat No 6,630,964) discloses a multi-standard channel decoder for real-time digital broadcast reception.
- The article "The Case for a Single-Chip Multiprocessor" by Olukotun discusses the advantages of multiprocessors.

5. Any inquiry concerning this communication or earlier communications from the examiner should be directed to John Manning whose telephone number is 703-305-0345. The examiner can normally be reached on M-F: 8:00 - 5:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, John W Miller can be reached on 703-305-4795. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

JM
March 19, 2005

JOHN MILLER
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